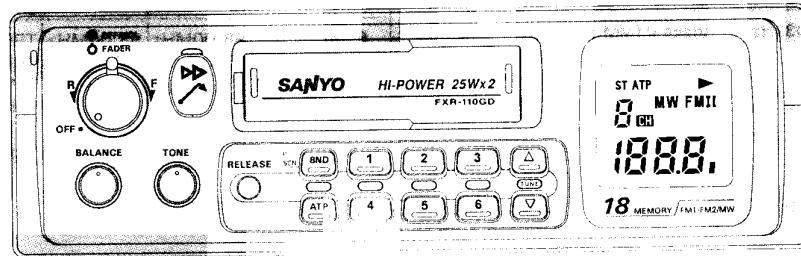


## SERVICE MANUAL COMPACT PANEL DETACHABLE DIN-SIZE FM-STEREO/MW ETR CASSETTE RECEIVER WITH AUTO-TRAVEL/PRESET TUNING

**FXR-110GD  
FXR-110GD/A**  
(GENERAL)



**PRODUCT CODE No.**  
FXR-110GD 147 589 22  
FXR-110GD/A 147 589 23

### Specifications

#### FM TUNER SECTION

Frequency Range .....87.5 MHz ~ 108 MHz  
Usable Sensitivity.....10dBf / 75ohms  
Frequency Response ( $\pm 3$  dB) .....40Hz ~ 12.5 kHz  
Signal to Noise ratio.....55 dB  
Selectivity ( $\pm 400$  kHz) .....65 dB  
Stereo Separation (1 kHz) .....30 dB

Maximum Output Power .....25W x 2 or  
7.5W x 4  
Load Impedance .....4 $\Omega$  (4 $\Omega$  ~ 8 $\Omega$  allowable)

#### MW TUNER SECTION

Frequency Range .....522 kHz ~ 1620 kHz  
Usable Sensitivity (S/N 20 dB) .....35 dB

#### GENERAL

Operating Voltage .....14.4V (11 ~ 16V allowable)  
Current Consumption .....6.0A  
Size (W X H X D) .....178 X 50 X 158 mm

#### CASSETTE DECK SECTION

Wow & Flutter (DIN) .....0.15%  
Fast Winding (C-60) .....90 sec  
Frequency Response (120 $\mu$ s) .....50 Hz ~ 14 kHz  
Cross Talk (1000 Hz) .....45 dB

Specification are subject to change without notice.

REFERENCE NO. SM750253

# ALIGNMENT PROCEDURES

- Power Supply DC 14.4V
- Signal generator output :  
 Modulation frequency : 400Hz (MW) : 1kHz (FM)  
 Modulation percentage 30% : 22.5kHz (FM)
- Reference output 500mW
- Signal Generator output level is in EMF.
- Signal application :  
 Antenna receptable through the dummy antenna
- Output meter connection : Across speaker or dummy load (4 ohms)
- Location of the components for alignment are shown in main part identification illustration.

## MW RF ALIGNMENT

Step	Signal	Frequency	Dial Set	Test Equipment	Adjustment
1	MW		522kHz	Connect a DC voltmeter to TP1 & common GND	Adjust T8 for voltage to be 1.2V
2	Through Dummy ANT (Fig.1)	603kHz	603kHz	Connect VTVM to output terminal	Tune T1, T3 RF coil for maximum output
3		999kHz	999kHz	Connect VTVM to output terminal	Tune T5, IF coil for maximum output
4		999kHz 30dBμ	999kHz	TP5 through 10K resistor to 5V. Connect a voltage meter to TP2 and ground	Adjust SVR2 between 2.5V to 4.5V

Rsg : Internal resistance of a signal generator

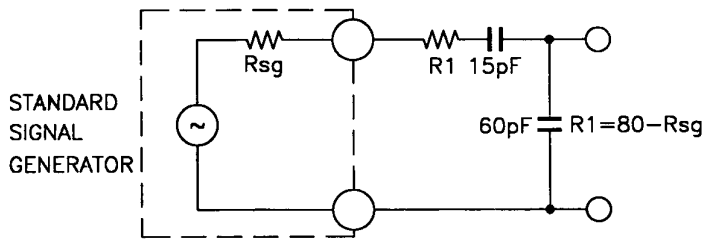


Fig. 1 Dummy Antenna for MW Alignment

Rsg : Internal resistance of a signal generator (50Ω)

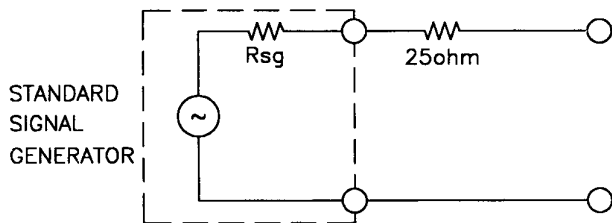


Fig. 2 Dummy Antenna for FM Alignment

## FM ALIGNMENT

Step	Signal Input	Frequency of signal Generator	Dial Setting of Radio	Test Equipment Connection	Adjustment	
1	Through Dummy ANT (Fig. 2)		108.0MHz	Connect DC voltmeter to TP1 & GND	Adjust L705 to 7.8V	
2		90.00MHz	90.00MHz	Connect VTVM to speaker output	Adjust T701 for maximum output (I.F.)	
3		90.00MHz	90.00MHz		Adjust L701, 703 & 704 for maximum output	
4		Repeat the step 2 until maximum output				
5		98.00MHz 60dBμ	98.00MHz	Connect a DC Voltmeter between TP3 and TP4	Adjust T6 to OV ± 20mV	
6		98.00MHz 21dBμ	98.00MHz	TP5 through 10K resistor to 5V. Connect a voltage meter to TP2 and ground	Adjust SVR1 to HIGH (5V)	

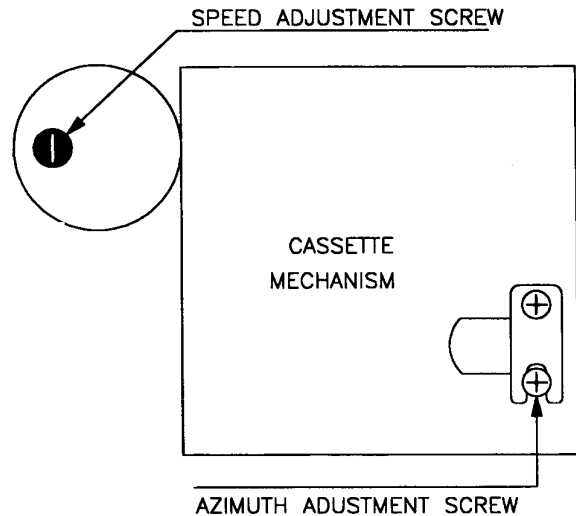
Note :  
 Open the L703 first, adjust T701, then adjust L701, L703 and L704.

## ALIGNMENT OF TAPE SPEED

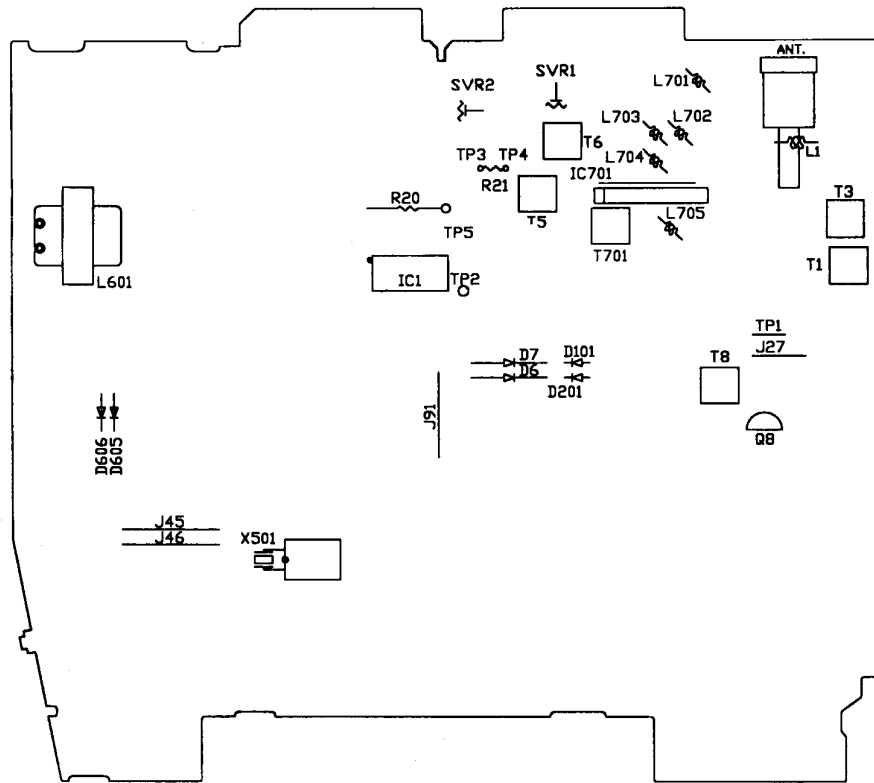
1. Insert 3kHz (MTT-111) standard test tape and set the unit at play mode.
2. Connect the Wow and Flutter Meter to speaker output.
3. Turn the speed adjustment screw to get  $3000 \pm 30\text{Hz}$ .

## ALIGNMENT OF HEAD AZIMUTH

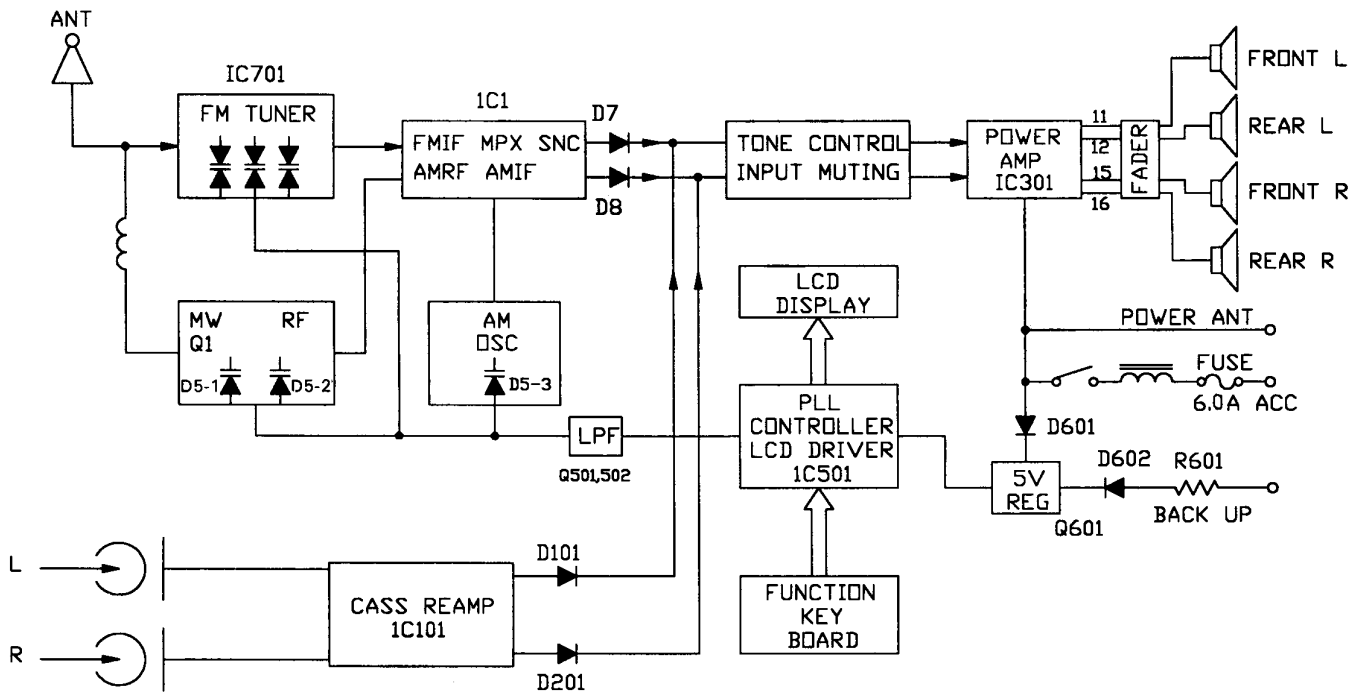
1. Insert a 10kHz (MTT255J) standard test and set the unit in play mode.
2. Tune the azimuth adjusting screw until you obtain maximum reading for both channel on the VTVM.



# MAIN PARTS IDENTIFICATION ILLUSTRATION



# BLOCK DIAGRAM



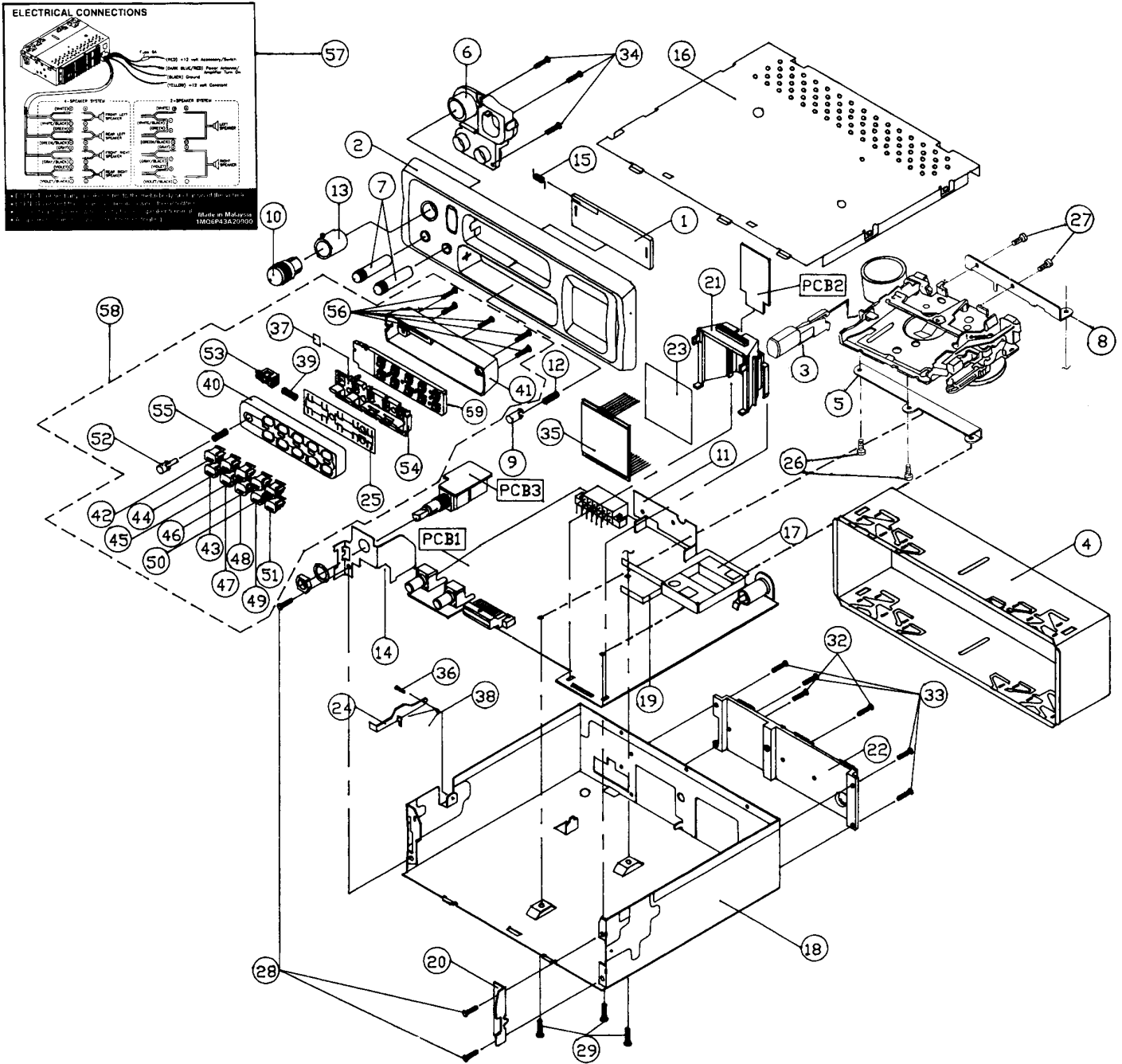


# PARTS LIST

Ref. No.	PART No.	DESCRIPTION	Q'ty	Ref. No.	PART No.	DESCRIPTION	Q'ty
<b>ASSY, PCB-W, LCD</b>				<b>ASSY, PCB-W, SWITCH</b>			
PCB2	641 006 4779	ASSY, PCB-W, LCD	1	FC302 TO FS302	641 006 4830	PC, JOINER, 3P-70MM	1
D607,608	408 035 3209	LED SLP-481C-51-ABY-T1	2	S601,VR303, 304,305	641 006 4816	VR, ROTARY	1
<b>ASSY, PCB-W, VR</b>							
PCB3	641 006 4786	ASSY, PCB-W, VR	1				
FC301 TO FS301	641 006 4823	PC, JOINER, 10P-80MM	1				

- NOTES:
1. Part orders must contain Model Number, Part Number and Description.
  2. Order quantity of screws and resistors must be multiple of 10 pcs.
  3. Regular type resistor and capacitor are omitted. Check the schematic diagram for these values.

# EXPLODED VIEW



# IC AND TRANSISTOR VOLTAGE CHART

IC	PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
		IC1	FM	5.3	0.3	0	5.2	0.1	8.3	1.2	4.2	0	4.2	4.2	0	4.2	8.3	0.1	8.2	4.4
MW	5.3		0.2	0	0	1.8	8.2	1.1	3.7	0	3.7	3.7	0	3.7	8.2	0	8.2	3.7	2.5	0.7
	20		21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36		
FM	4.1		4.7	3.2	3.3	3.3	3.3	0	0	3.3	3.2	3.6	3.4	0.7	0.1	0	4.1	0		
	MW	3.7	4.7	2.8	2.9	3.3	3.3	0	0	3.3	3.3	3.3	3.0	0.6	3.7	2.2	3.5	2.9		

IC	PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
IC101		1.3	0.8	2.3	13.9	0	2.3	0.8	1.3									
IC301		13.9	5.1	5.2	4.9	0	5.1	5.2	5.2	13.9	13.9	6.2	6.2	0	0	6.2	6.2	13.9
IC701		8.0	3.9	8.0	0.7	0	2.2	1.6	6.6	5.2								

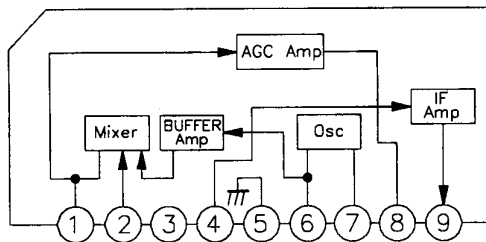
PIN	TR	Q9	Q301	Q401	Q501	Q502	Q503	Q504	Q505	Q506	Q507	Q508	Q509	Q510	Q515	Q516	Q601	Q702
		B	ON	3.8	0.6	0.6	1.2	0.7	4.8	5.4	4.9	0	0	0	8.9	0.9	0	0.6
OFF	0.7		0	0	—	—	0	0	0	2.3	0.1	0.1	—	8.2	5.0	0	—	—
C	ON	8.2	0	0	*	*	0	0	0	0	0	0.1	13.5	8.1	4.9	0	13.2	6.9
	OFF	8.2	0	0	—	—	0.1	0.1	2.8	0	0	0	—	0	0	5.1	—	—
E	ON	3.2	0	0	0.7	0	0	0	0	0	0	0	8.2	8.2	4.9	0	5.6	0
	OFF	0.2	0	0	—	—	0	0	0	0.6	0	0	—	8.3	5.1	0	—	—

PIN	TR	Q1	Q8
D		0.2	0
G		0	0
S		0.1	1.5
B		0.8	
C		8.2	

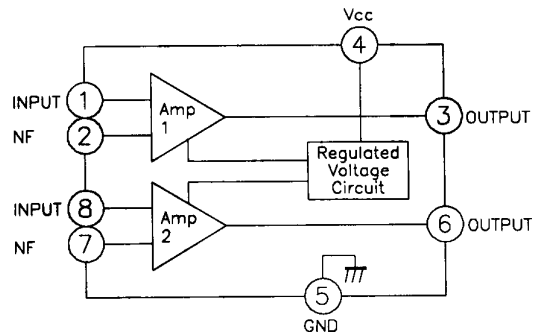
\* : FM 1.2~7.8  
: MW 1.2~7.2

## IC BLOCK DIAGRAM

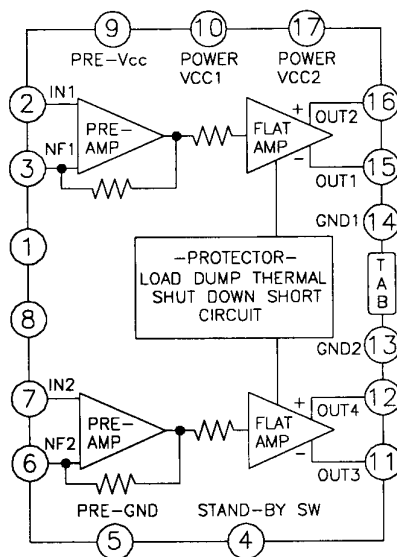
LA 3161



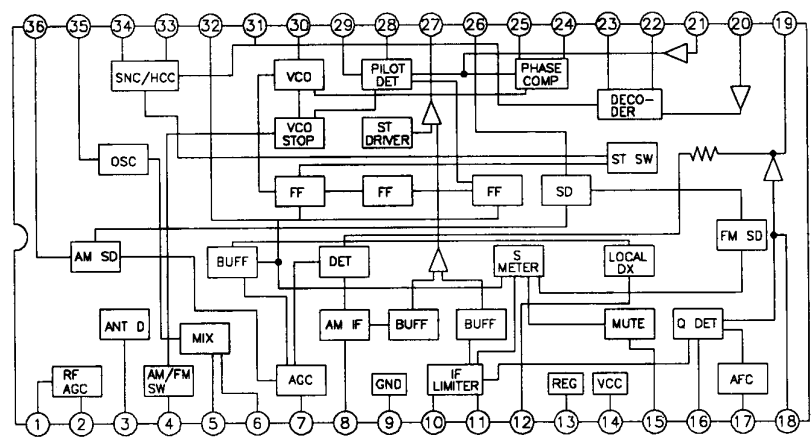
AN7254



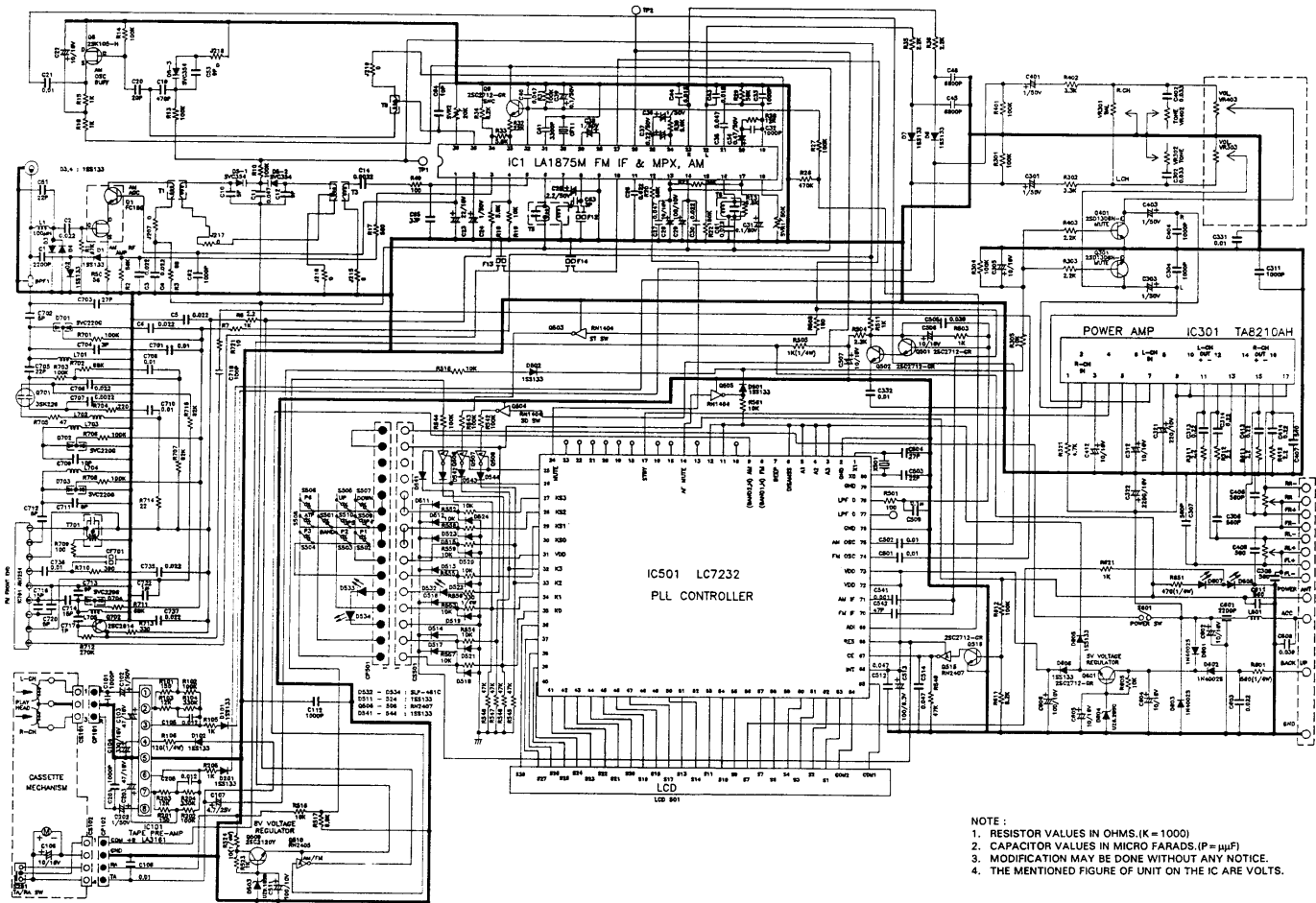
TA 8210AH



LA 1875M



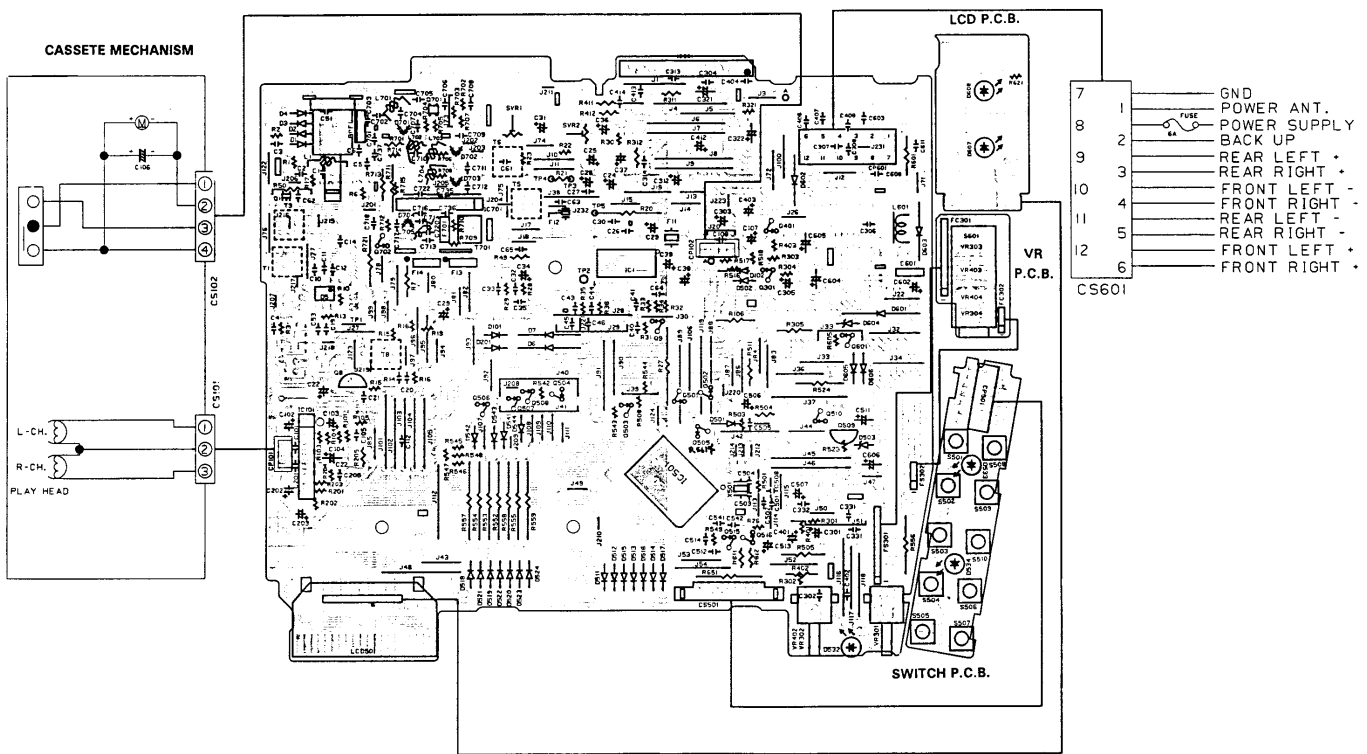
SCHEMATIC DIAGRAM



- NOTE :
1. RESISTOR VALUES IN OHMS.(K = 1000)
  2. CAPACITOR VALUES IN MICRO FARADS.(P = μF)
  3. MODIFICATION MAY BE DONE WITHOUT ANY NOTICE.
  4. THE MENTIONED FIGURE OF UNIT ON THE IC ARE VOLTS.

WIRING DIAGRAM

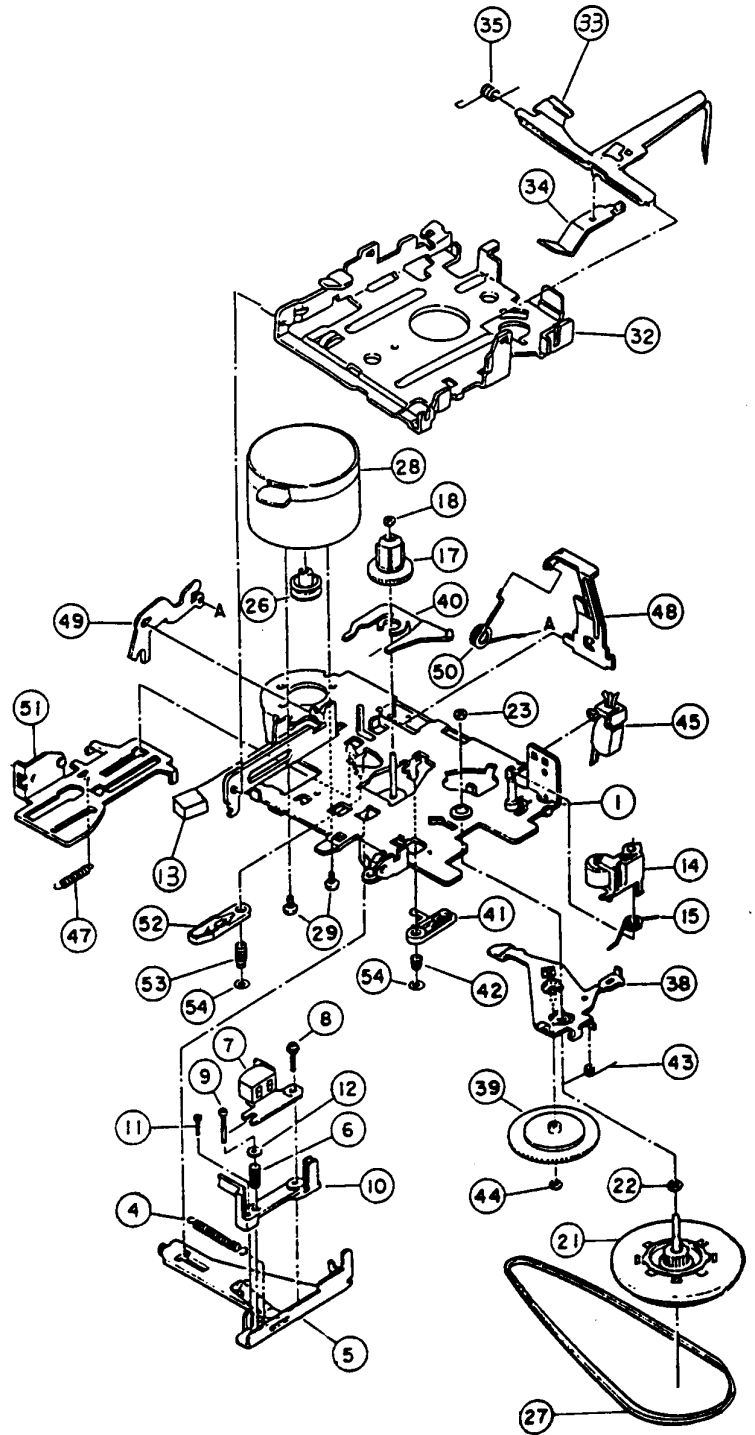
MAIN P.C.B. BOTTOM





**PARTS LIST (CASSETTE MECHANISM) — EXPLODED VIEW**

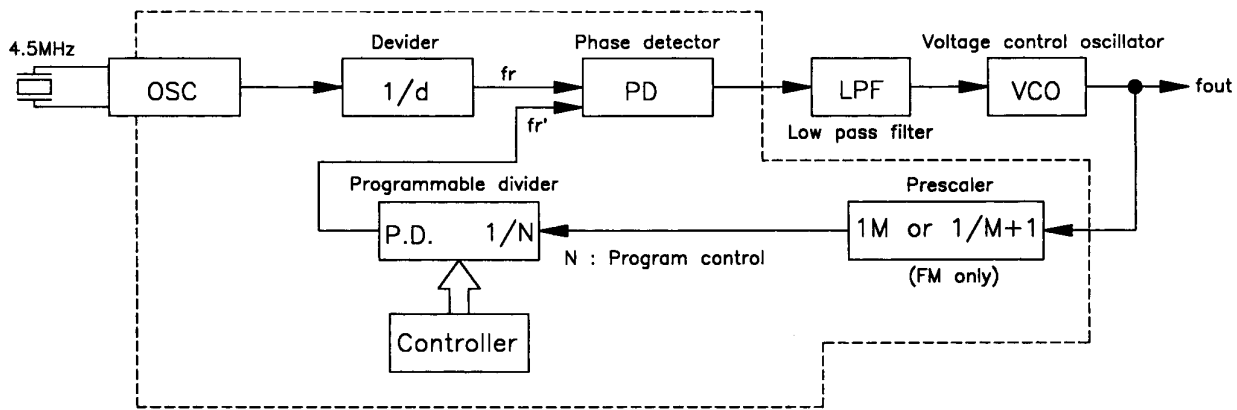
Ref. No.	PART No.	DESCRIPTION	Q'ty
<b>CASSETTE MECHANISM (641 005 4909)</b>			
	641 005 4909	ASSY, MECHA TN-301NX-258	1
1	641 002 5169	CHASSIS ASSY	1
4	641 001 9045	HEAD PANEL SP	1
5	641 001 9021	HEAD PANEL	1
6	641 001 9014	AZIMUTH SPRING	1
7	641 005 4916	HD.P-7442BS-3453	1
8	641 001 9281	TAMS SCREW 2X9	1
9	641 001 9298	AZIMUTH SC M2X10	1
10	641 001 9038	HEAD BASE	1
11	641 000 6076	CAMERA SCR 2X5.5	1
12	641 000 6793	WAS. 2.1X5X0.2	1
13	641 001 9007	ANTI-VIB MAT	1
14	641 001 8963	PINCH ROLLER ASSY	1
15	641 001 9069	PINCH ROLLER SP	1
17	641 001 8970	REEL GEAR ASSY	1
18	641 001 9274	HW(10.3X14.2X.4)	1
21	641 001 8987	FLYWHEEL ASSY	1
22	641 002 5190	P.WAS 2.1X3.5X.3	1
23	641 001 9328	H.W. (C1.5X3.2X.5)	1
26	641 004 1794	MOTOR PULLEY	1
27	641 001 9076	MAIN BELT	1
28	641 005 4923	MOTOR, EG530AD2FS	1
29	632 547 2966	M2.6X3 PAN M/C SC	2
32	641 001 9120	CASS CASE	1
33	641 002 4933	KICK PLATE	1
34	641 001 9106	PACK HOLDER SP	1
35	632 227 7694	KICK PLATE SP	1
38	641 001 8994	GEAR PLATE ASSY	1
39	641 001 9137	CAM GEAR	1
40	641 001 9144	SENSOR	1
41	641 001 9175	G. LOCK LEVER	1
42	641 001 9151	G. LOCK LEV SP	1
43	641 001 9168	GEAR PLATE SP	1
44	641 001 9267	P.W (C1.2X3.8X.3)	1
45	641 001 9250	LEAF SW	1
47	641 001 9205	FUNC. LEVER SP	1
49	641 001 9212	LIFT UP LEVER	1
48	641 001 9229	PUSH PLATE	1
50	641 001 9243	REVERSE SPRING	1
51	641 001 9236	FUNCTION LEVER	1
52	641 001 9182	FF LOCK LEVER	1
53	641 001 9199	LOCK LEVER SP	1
54	641 001 9304	H.WASH 2.1X5X0.3	2



- NOTES: 1. Part orders must contain Model Number, Part Number and Description.  
 2. Order quantity of screws and resistors must be multiple of 10 pcs.

# CIRCUIT OPERATION DESCRIPTION

## 1. BASIC OPERATION OF PLL FREQUENCY SYNTHESIZER



The illustration above is a block diagram which is a fundamental PLL frequency synthesizer.

In order to obtain reference frequency  $f_r$ , the frequency of 4.5MHz generated from a crystal oscillator (OSC) is passed into a divider circuit of  $1/d$ .

This  $f_r$  is compared with  $f_r'$ , and runs through phase detector (PD) and low pass filter (LPF) to be inverted to direct-current signal, which is then applied as varicap voltage of voltage control oscillator (VCO), thereby controlling the oscillation frequency.

This oscillation frequency  $f_{out}$  is divided down to  $1/N$  by programmable divider (PD), so that one closed loop is fixed in the relation of

$$f_{out} = f_r \times N$$

therefore, the operation of PLL is stabilized.

In case of automatic channel selection, the dividing ratio  $N$  is altered by the PD by a command from controller, and  $f_{out}$  is changed accordingly.

### Programmable divider

Since the oscillation frequency of VCO is very high as compared with  $f_r$ , it is divided down to  $1/N$  (in the case of MW) to decrease the difference from  $f_r$  in this circuit.

### Phase detector

This is a circuit to detect the difference in frequency and phase between reference frequency  $f_r$  and comparison frequency  $f_r'$  in terms of pulses.

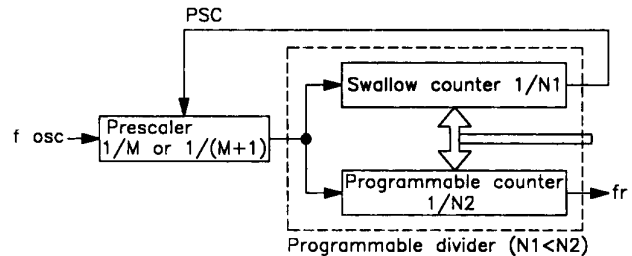
### Low pass filter

This circuit is intended to vary and fix the output voltage in order to deliver a varicap voltage necessary for desired VCO frequency, on the basis of the output of the phase detector.

### Prescaler

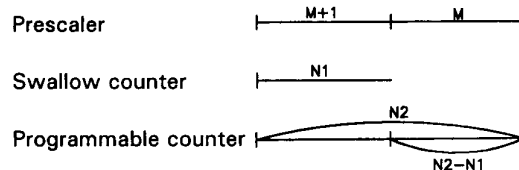
The local oscillation frequency in FM is higher than the operating speed of the programmable divider of PLL, thereby opposing to accurate operation. To avoid this, the local oscillation frequency is preliminarily divided down in this circuit to a proper frequency permitting reliable operation of the programmable divider.

Pulse swallow count system is employed. A couple of programmable divider (swallow counter and programmable counter) can be selected.



$$f_{osc} = \{(M+1)N_1 + M(N_2 - N_1)\} f_r'$$

$$= (MN_2 + N_1) f_r'$$



The prescaler at first starts the frequency division with the ratio  $M+1$ . Then the swallow counter and the programmable counter starts counting simultaneously. When  $N_1$  inputs are applied, the swallow counter stops counting. Then the frequency division ratio of the prescaler is switched to  $M$ . Programmable counter continues to count and stops when the input reaches  $N_2$ . The frequency division ratio of the prescaler switches back to  $M+1$  and swallow counter and the programmable counter start to count again.

FM reception employs the pulse swallow count system. MW reception does not employ the pulse swallow count system but employs the direct frequency division system and so only programmable counter is operated.

## 2. GENERAL DESCRIPTION OF LOGIC IC (IC501)

### a) IC801 LC7232-8424

This IC includes PLL and controller is a C-MOS LSI for digital tuning of FM/MW PLL frequency synthesizer system and controls such functions as FM/MW automatic channel selections, preset memory and frequency digital display driver. It is packed in a 80-pin flat package.

## 3. AUTOSTOP

If counter start, when high level signal is applied to SD terminal (Q504 base). Then IF frequency became  $10.7\text{MHz} \pm 30\text{kHz}$  at FM or  $450\text{kHz} \pm 3\text{kHz}$  at MW. When SD and IF is agreed radio auto search tuning stops.

# CIRCUIT OPERATING DESCRIPTION

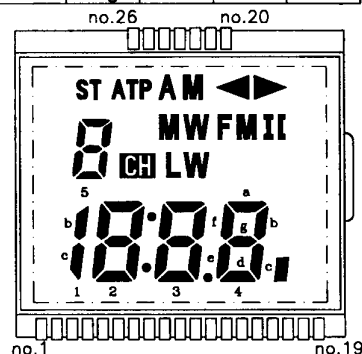
DESCRIPTION (LC7232-8424)

PIN NO	SYMBOL		FUNCTIONAL EXPLANATION																								
	IN	OUT																									
1	XIN		Input side of inverter for OSC																								
2	GND																										
3	AREA3		Key return signal input																								
4	AREA2		Key return signal input																								
5	AREA1		Key return signal input																								
6	DIS AMSS		Key return signal input																								
7		BEEP	BEEP Signal output																								
8		BAND 1	<table border="1"> <thead> <tr> <th>PIN</th> <th>BAND</th> <th>FM</th> <th>MW</th> <th>LW</th> <th>FM* SDK</th> </tr> </thead> <tbody> <tr> <td>BAND 1</td> <td></td> <td>I</td> <td>O</td> <td>O</td> <td>I</td> </tr> <tr> <td>BAND 2</td> <td></td> <td>O</td> <td>I</td> <td>O</td> <td>I</td> </tr> <tr> <td>VF</td> <td></td> <td>I</td> <td>I</td> <td>I</td> <td>O</td> </tr> </tbody> </table>	PIN	BAND	FM	MW	LW	FM* SDK	BAND 1		I	O	O	I	BAND 2		O	I	O	I	VF		I	I	I	O
PIN	BAND	FM		MW	LW	FM* SDK																					
BAND 1		I		O	O	I																					
BAND 2		O	I	O	I																						
VF		I	I	I	O																						
9		BAND 2																									
10		VF																									
11	DIS DOLBY		Key return signal input																								
12	DIS MTL		Key return signal input																								
13	SDK	—	SDK signal output																								
14		MUTE	MUTE signal output																								
15		MODE 1	<table border="1"> <thead> <tr> <th></th> <th>TAPE</th> <th>FM</th> <th>AM</th> <th>AM:MW LW</th> </tr> </thead> <tbody> <tr> <td>MODE 1</td> <td>O</td> <td>I</td> <td>I</td> <td></td> </tr> <tr> <td>MODE 2</td> <td>I</td> <td>O</td> <td>I</td> <td></td> </tr> </tbody> </table>		TAPE	FM	AM	AM:MW LW	MODE 1	O	I	I		MODE 2	I	O	I										
	TAPE	FM		AM	AM:MW LW																						
MODE 1	O	I	I																								
MODE 2	I	O	I																								
16		MODE 2																									
17		STBY	AMP STBY output																								
18		TA MUTE	TAPE MUTE output																								
19		LOUD.	LOUDNESS signal output																								
20		LO	LO signal output																								
21		DOLBY	DOLBY signal output																								
22		AMSS	AMSS signal output																								
23		MO/MTL	MO/MTL signal output																								
24		RA MUTE	RA MUTE signal output																								
25		KS5	Key matrix return signal output 5																								
26		KS4	Key matrix return signal output 4																								
27		KS3	Key matrix return signal output 3																								
28		KS2	Key matrix return signal output 2																								
29		KS1	Key matrix return signal output 1																								
30		KS0	Key matrix return signal output 0																								
31	VDD		VDD 5V																								
32	K3		Key matrix return signal output 3																								
33	K2		Key matrix return signal output 2																								
34	K1		Key matrix return signal output 1																								
35	K0		Key matrix return signal output 0																								
36		S28	LCD19 output for LCD																								
37		S27	LCD18 output for LCD																								
38		S26	LCD17 output for LCD																								
39		S25	LCD16 output for LCD																								
40		S24	LCD15 output for LCD																								
41		S23	LCD14 output for LCD																								
42		S22	LCD13 output for LCD																								
43		S21	LCD12 output for LCD																								
44		S20	LCD11 output for LCD																								
45		S19	LCD10 output for LCD																								
46		S18	LCD9 output for LCD																								
47		S17	LCD20 output for LCD																								
48		S16	NC																								
49		S15	NC																								
50		S14	LCD24 output for LCD																								
51		S13	LCD21 output for LCD																								
52		S12	NC																								
53		S11	LCD22 output for LCD																								

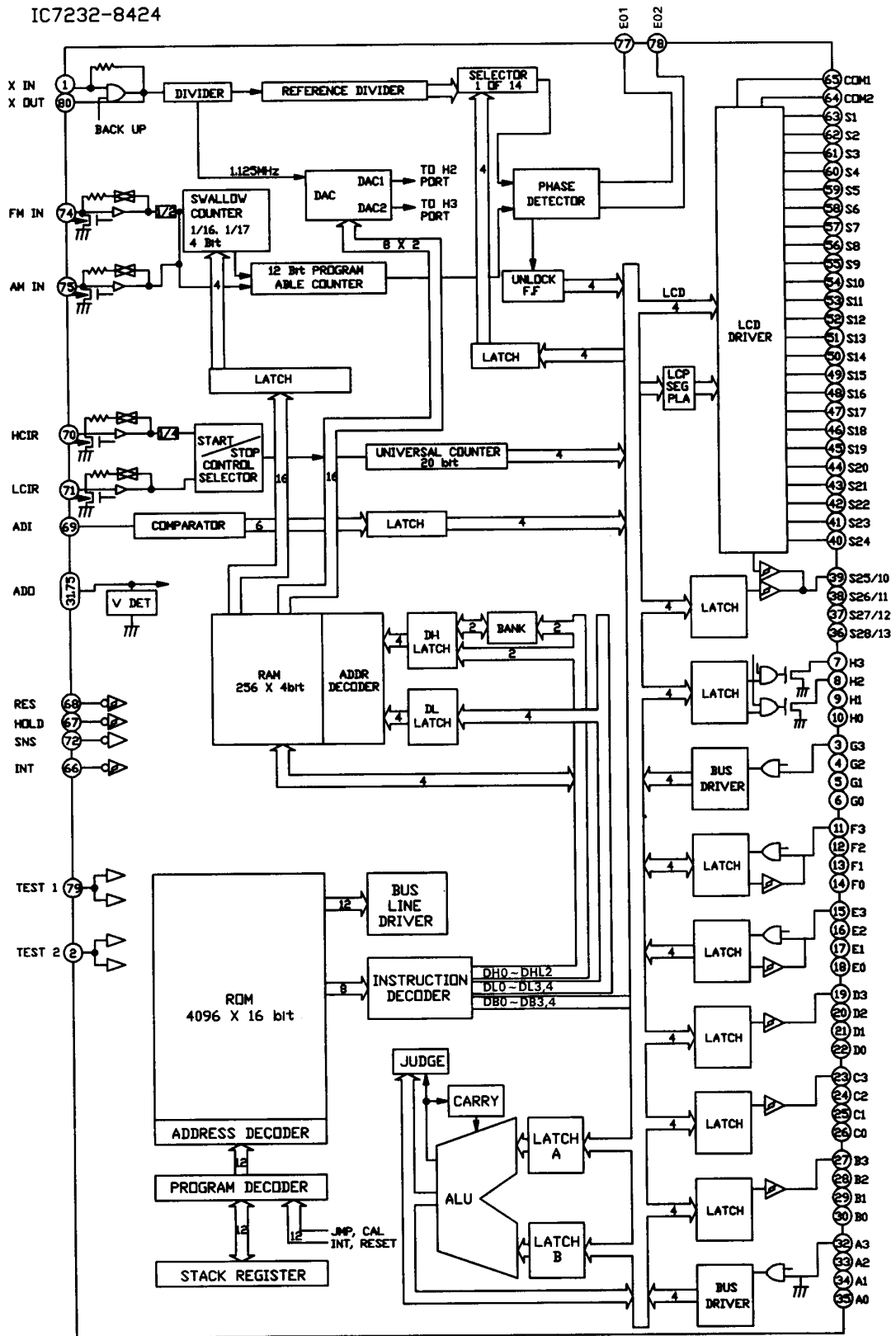
PIN NO	SYMBOL		FUNCTIONAL EXPLANATION
	IN	OUT	
54		S10	LCD23 output for LCD
55		S9	LCD25 output for LCD
56		S8	NC
57		S7	LCD8 or 26 output for LCD
58		S6	LCD7 output for LCD
59		S5	NC
60		S4	LCD6 output for LCD
61		S3	LCD5 output for LCD
62		S2	LCD4 output for LCD
63		S1	LCD1 output for LCD
64		COM2	COMMON signal 2 output for LCD
65		COM1	COMMON signal 1 output for LCD
66	INT		VDD 5V
67	CE	—	ChipEnable (+5V)
68	RES		RESET
69	ADI		Signal meter level input
70	FM IF		FM IF input
71	AM IF	—	AM IF input
72	SNS		VDD 5V
73	VDD		VDD 5V
74	FM in		FM OSC input
75	AM in		AM OSC input
76	GND		GND
77		E01	Phase detector output 1
78		E02	Phase detector output 2
79	GND		
80		Xout	Output side of inverter for OSC

## LCD SEGMENT & COMMON LINE

Pin	COM1	COM2	Pin	COM1	COM2
1	COM1		14	3 d	3 c
2		COM2	15	3 a	dot
3	5 f	5 b	16	4 f	4 b
4	5 e	5 g	17	4 e	4 g
5	5 d	5 c	18	4 d	4 c
6	5 a	CH	19	4 a	█
7	LW		20	2 f	2 b
8	MW	FM	21		1 bc
9	2 e	2 g	22	◀	◻
10	2 d	2 c	23	▶	◻
11	2 a	•	24		ATP
12	3 f	3 b	25		ST
13	3 e	3 g	26	AM	



# IC BLOCK DIAGRAM



# SANYO

SEPT/'98/1100

Printed in Malaysia

SANYO Electric Co., Ltd.  
Osaka, Japan.