Ordering number:ENN2668A

Thick Film Hybrid IC

STK4132 Ⅱ

2ch AF Power Amplifier (Split Power Supply) (20W + 20W min, THD = 1%)

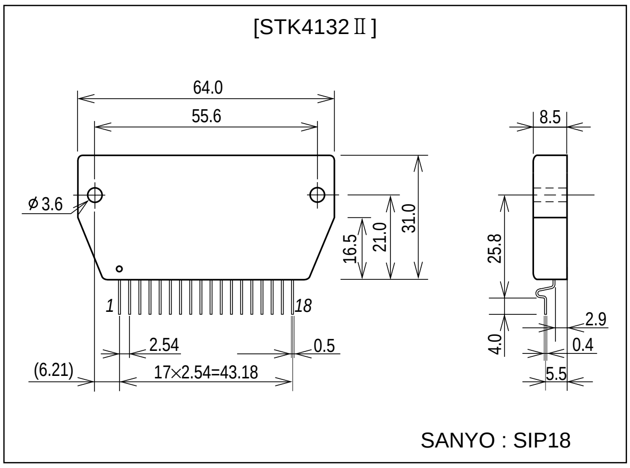
Features

- Pin compatible with the STK4102 Ⅱ and STK4101V series (hith-grade type) over the output range 6 to 50W for easy interchangability
- Small-sized package with the same pin assignment as the STK4101 Ⅱ series
- Built-in muting circuit to cut off spurious shock noise
- 125°C guaranteed high temperature operation allows greatly reduced heat sink size
- Excellent low-cost performance

Package Dimensions

unit:mm

4083



Specifications

Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		±34.5	V
Thermal resistance	θ j-c		3.0	˚C/W
Junction temperature	Tj		150	˚C
Operating substrate temperature	Tc		125	˚C
Storage temperature	Tstg		–30 to +125	˚C
Available time for load short-circuit	t_s	V_{CC}=±23V, R_L=8Ω, f=50Hz, P_O=20W	2	s

Recommended Operating Conditions at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		±23	V
Load resistance	R_L		8	Ω

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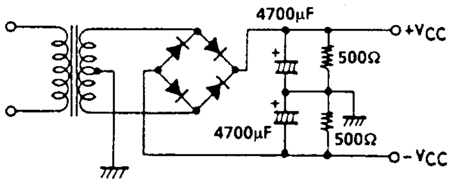
Operating Characteristics at Ta = 25˚C, V_{CC}=±23V, R_L=8Ω (non-inductive load), Rg=600Ω, VG=40dB

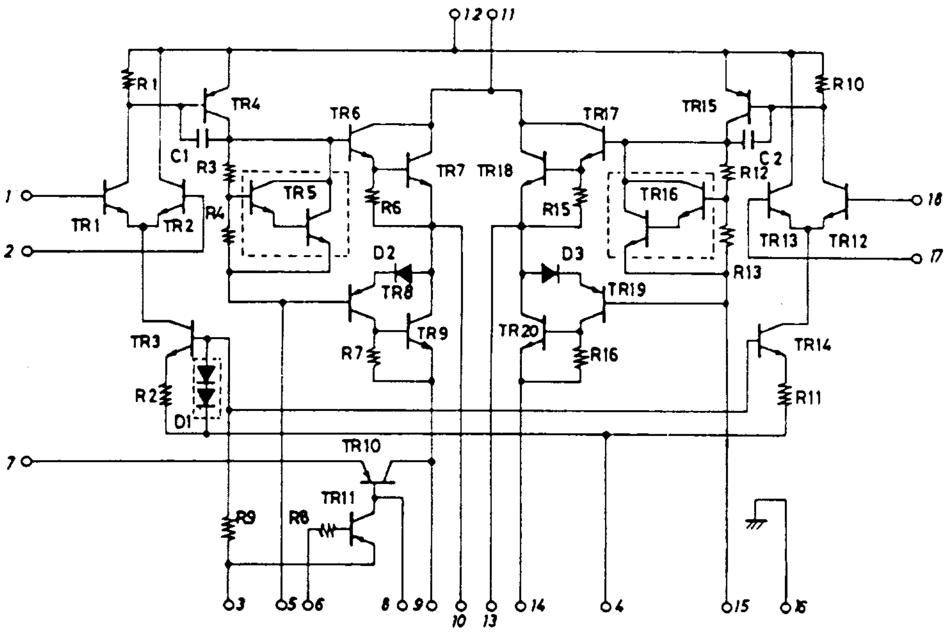
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	V_{CC}=±28V	20	40	100	mA
Output power	P_O1	THD=0.4%, f=20Hz to 20kHz	20			W
	P_O2	V_{CC}=±20V, THD=1.0%, R_L=4Ω, f=1kHz	20			W
Total harmonic distortion	THD	P_O=1.0W, f=1kHz			0.3	%
Frequency response	f_L, f_H	P_O=1.0W, $^{+0}_{-3}$ dB		20 to 50k		Hz
Input resistance	r_i	P_O=1.0W, f=1kHz		55		kΩ
Neutral voltage	V_N	V_{CC}=±50.5V	–70	0	+70	mV
Output noise voltage	V_{NO}	V_{CC}=±28V, Rg=10kΩ			1.2	mVrms
Muting voltage	V_M		–2	–5	–10	V

Note.
All tests are made using a constant-voltage supply unless otherwise specified.
Available time for load short-circuit and output noise voltage are measured using the transformer supply specified below.
The output noise voltage is the peak value of an average-reading meter with an rms value scale (VTVM). A regulated AC supply (50Hz) should be used to eliminate the effects of AC primary line flicker noise.

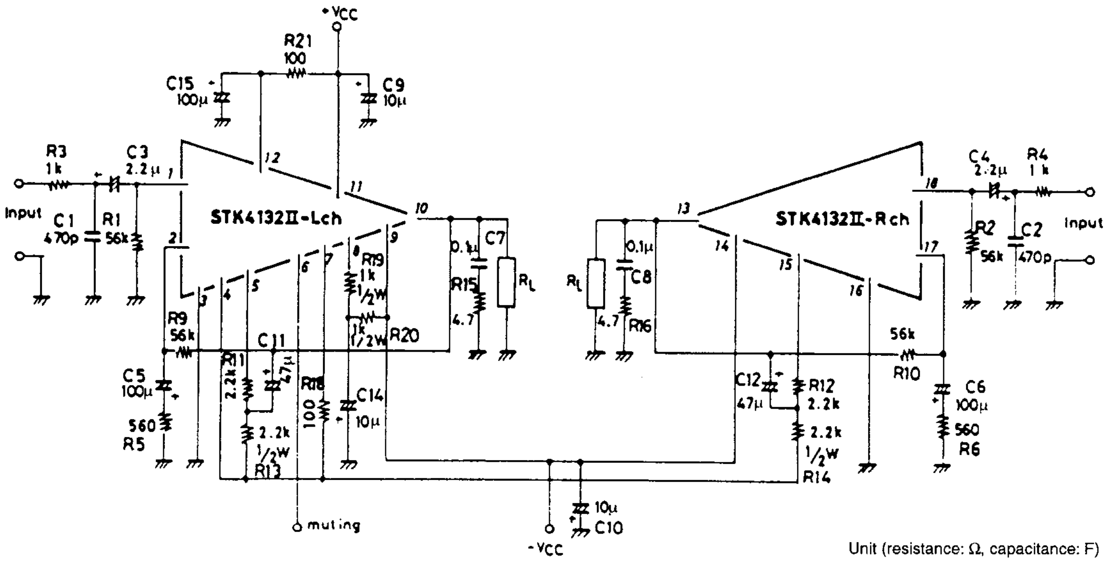
Specified Transformer Supply (RP-25 or Equivalent)



Equivalent Circuit

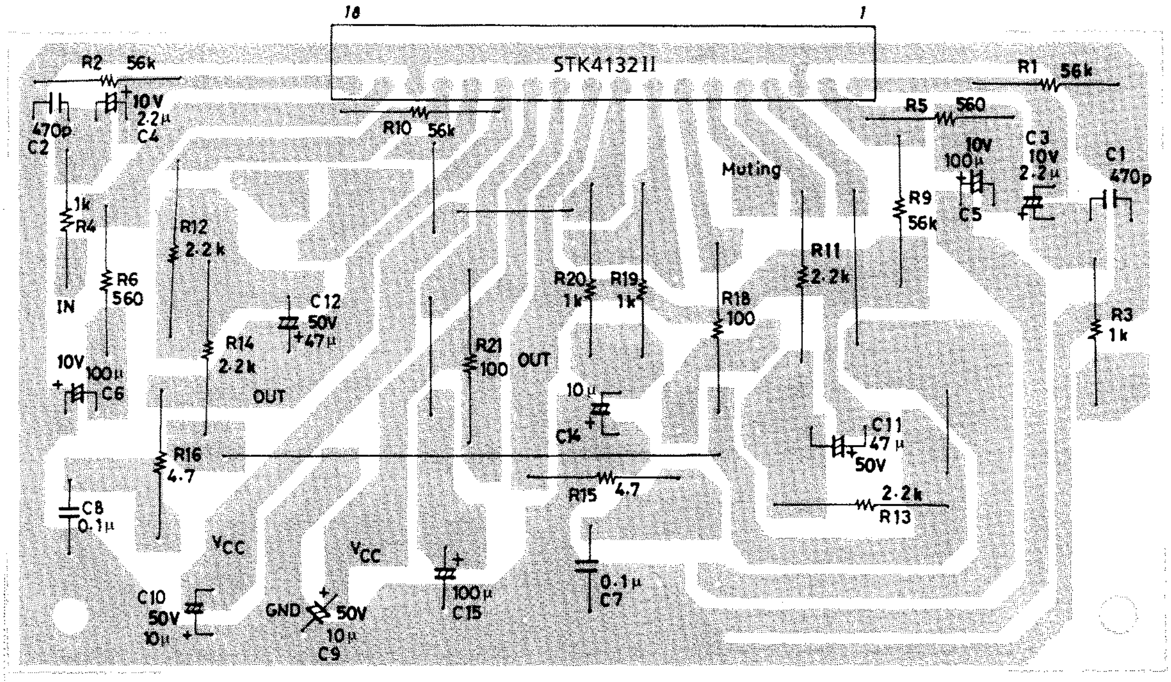


Sample Application Circuit (20W min, 2-Channel, AF Power Amplifier)



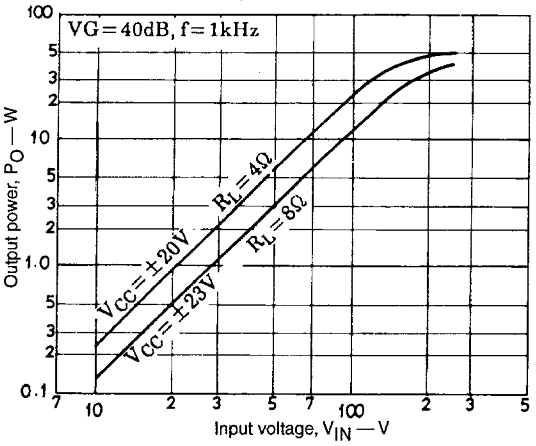
Unit (resistance: Ω, capacitance: F)

Sample Application Circuit PCB Layout (Copper Foil Surface)

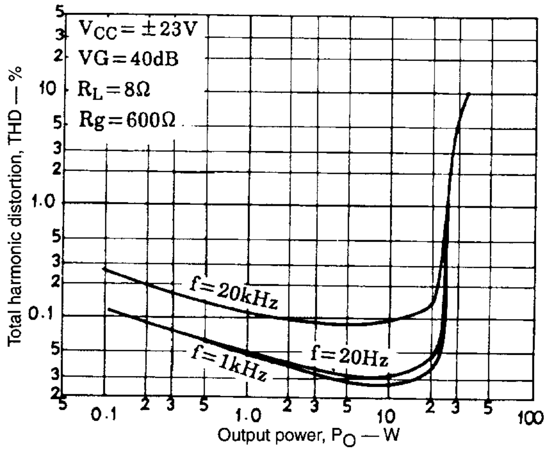


50 × 100mm²
Unit (resistance: Ω; capacitance: F)

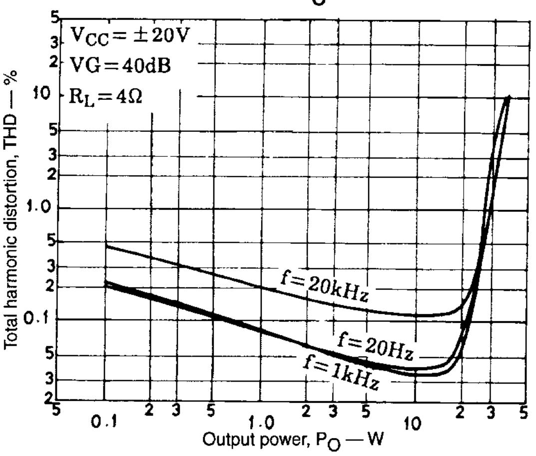
P_O — V_{IN}



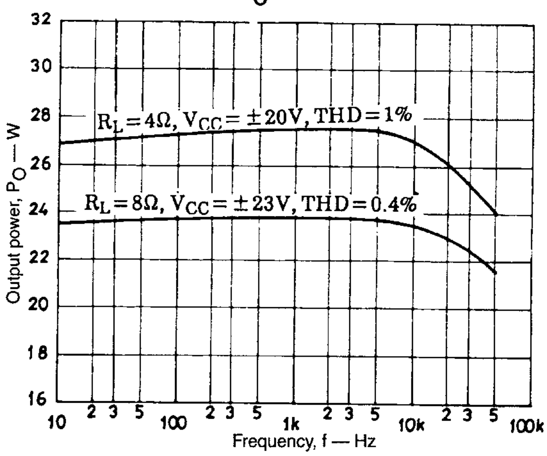
THD — P_O



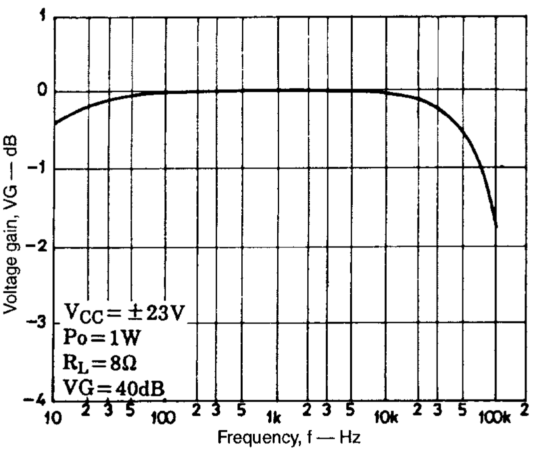
THD — P_O



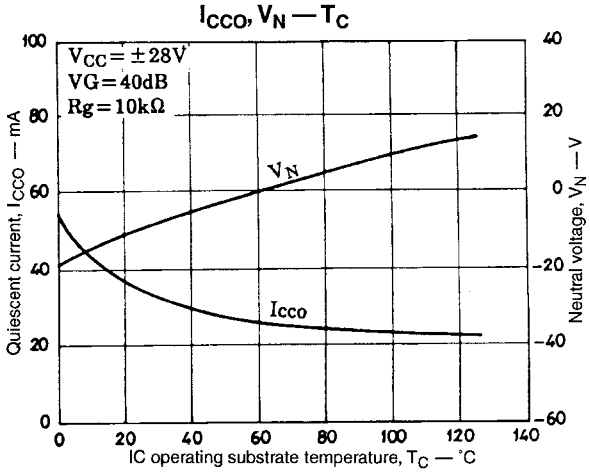
P_O — f



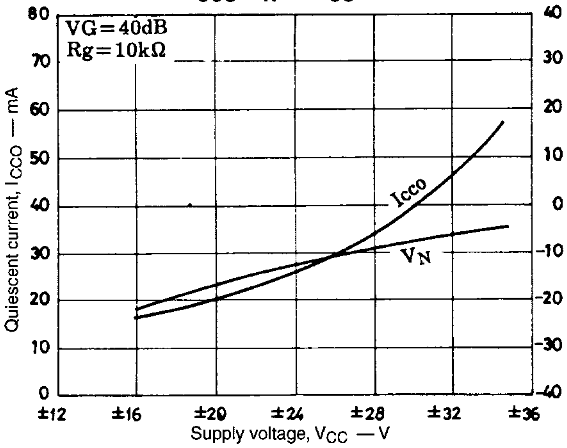
VG — f



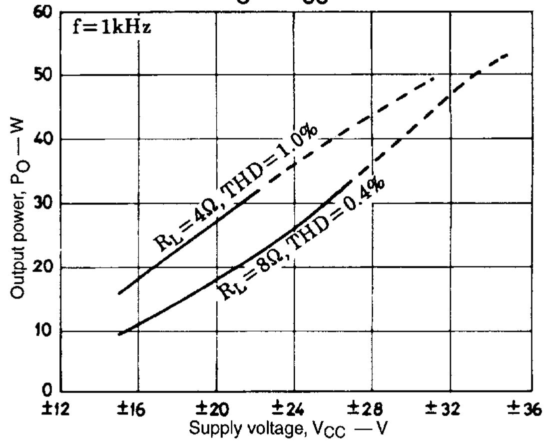
I_{CCO}, V_N — T_C

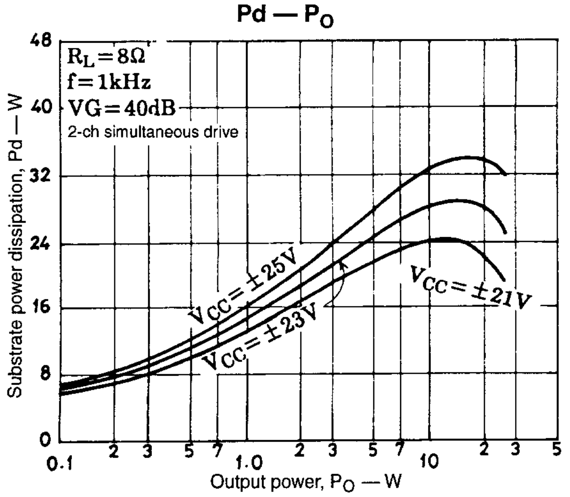


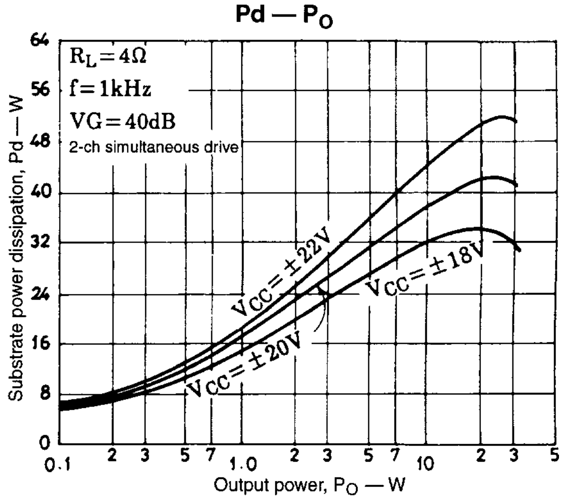
I_{CCO}, V_N — V_{CC}

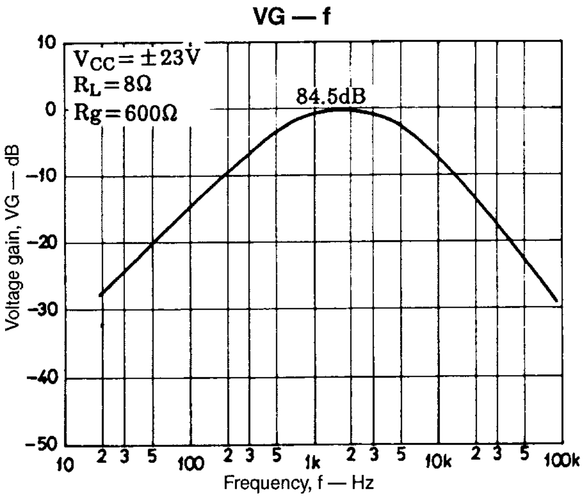


P_O — V_{CC}

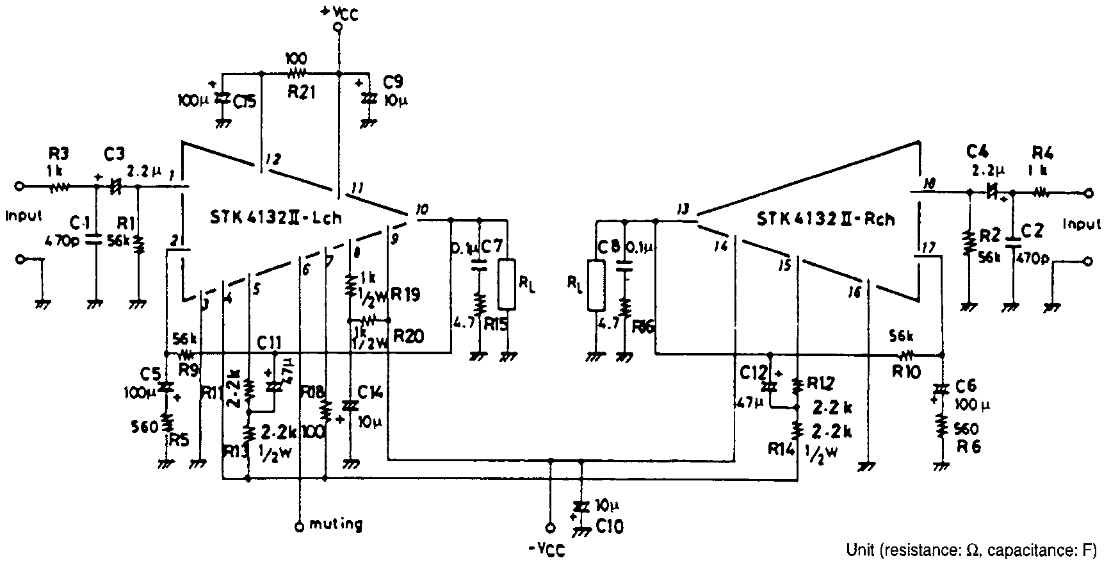



Pd — PO
RL=8Ω
f=1kHz
VG=40dB
2-ch simultaneous drive
VCC=±25V
VCC=±23V
VCC=±21V
Substrate power dissipation, Pd — W
Output power, PO — W
48
40
32
24
16
8
0
0.1
2
3
5
7
1.0
2
3
5
7
10
2
3
5


Pd — PO
RL=4Ω
f=1kHz
VG=40dB
2-ch simultaneous drive
VCC=±22V
VCC=±20V
VCC=±18V
Substrate power dissipation, Pd — W
Output power, PO — W
64
56
48
40
32
24
16
8
0
0.1
2
3
5
7
1.0
2
3
5
7
10
2
3
5


VG — f
VCC=±23V
RL=8Ω
Rg=600Ω
84.5dB
Voltage gain, VG — dB
Frequency, f — Hz
10
0
–10
–20
–30
–40
–50
10
2
3
5
100
2
3
5
1k
2
3
5
10k
2
3
5
100k

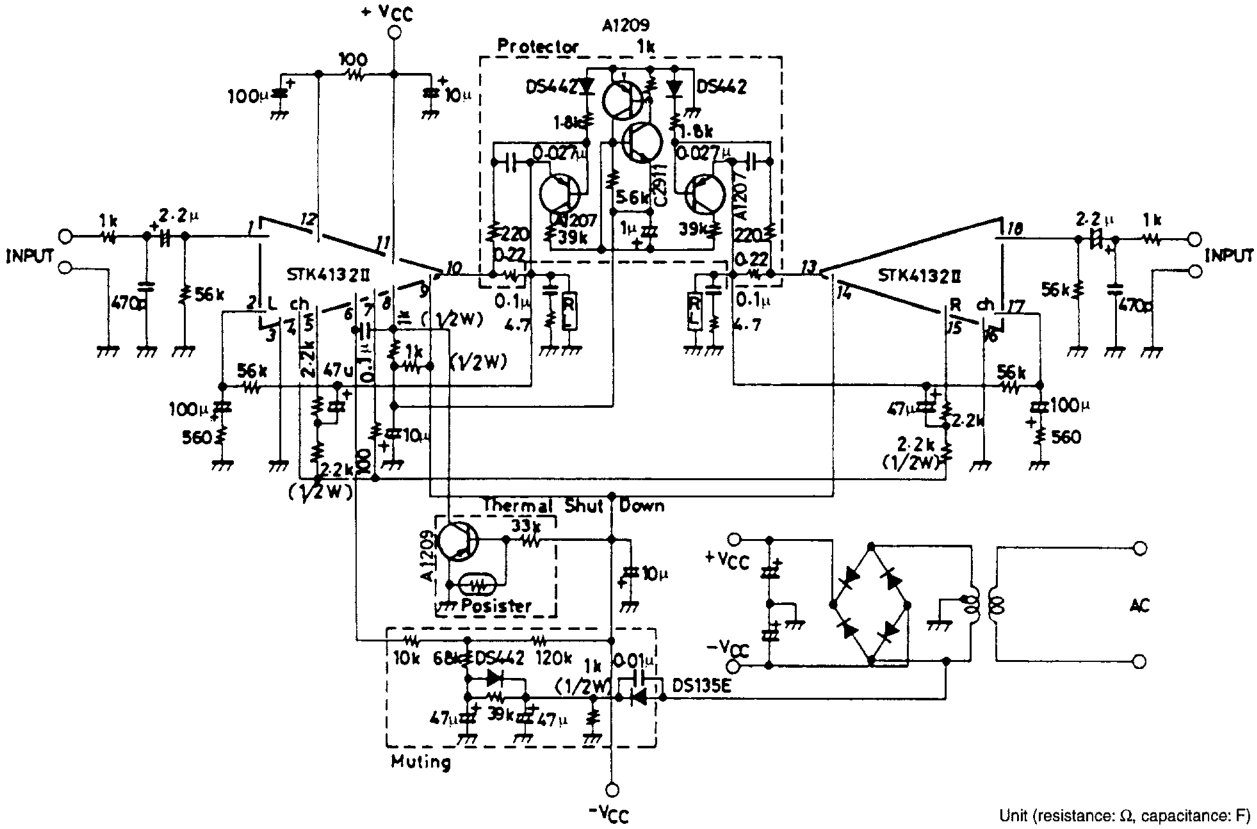
External Component Description



Unit (resistance: Ω, capacitance: F)

C1, C2	Input filter capacitors. These, together with R3 and R4, form filters to reduce high-band noise.
C3, C4	Input coupling capacitors. For DC blocking. Since capacitor reactance becomes larger at lower frequencies, the output noise can be adversely affected by signal source resistance-dependent 1/f noise. In this case, a lower rectance value should be chosen. In order to remove pop noise at power-on, larger values of capacitance should be chosen for C3 and C4, which determin the input time constant, and smaller values for C5 and C6 in the NF circuit.
C5, C6	NF capacitors. These determine the low-side cutoff frequency. $f_L = \frac{1}{2\pi \times C5 \times R5}$ [Hz] A large values should be chosen for C5 to maintain voltage gain at low frequencies. However, because this would tend to increase the shock noise at power-on, a values larger than absolutely necessary should be avoided.
C15	Decoupling capacitors. This removes shock noise and ripple voltage from the supply.
C11, C12	Bootstrap capacitors. If these capacitors are made small, then the total harmonic distortion at low frequencies increases significantly.
C9, C10	Oscillation prevention capacitors. These should be inserted as close as possible to the IC supply pins to reduce supply impedance and hence provide stable IC operation. Electolytic capacitors are recommended.
C14	Ripple filter capacitor. This forms a ripple filter in combinatin with internal transistor TR10.
C7	Oscillation prevention capacitors. Mylar capacitors are recommended for their excellent thermal and frequency characteristics.
R3, R4	Input filter resistors.
R1, R2	Input bias resistors. These are used to bias the input pins at aero potential. The input impedance is largely determined by this resistance.
R5, R9 (R6, R10)	Voltage-gain VG setting resistors. VG=40dB is recommended using R5, R6=560Ω, and R9, R10=56kΩ. Gain adjustments are best made using R5 and R6. If gain adjustments are made using R5 and R6, then set R1, R2=R9, R10 to maintain V_N balance stability.
R11, R13 (R12, R14)	Bootstrap resistors. These resistors determine the quiescent current. Values of 2.2kΩ and 2.2kΩ are recommended.
R21	Ripple filter tesistor. This resistor performs as predriver transistor limiting resistor during load short circuits.
R18	Clipping plus/minus balance resistor.
R19, R20	Ripple filter resistors. When muting transistor TR11 is on, current flows from ground through TR11 to $-V_{CC}$. Values of 1kΩ (0.5W) and 1kΩ (0.5W) are recommended.
R15, R16	Oscillation prevention resistors.

Sample Application Circuit (Protection and Muting Circuit)



Unit (resistance: Ω, capacitance: F)

Heatsink Design

The total STK4132Ⅱ device power dissipation for a continuous sine wave signal is shown in figures 1 and 2. The maximum dissipation is 29.2W for R_L=8Ω, and 42.8W for R_L=4Ω (2-channel simultaneous drive).

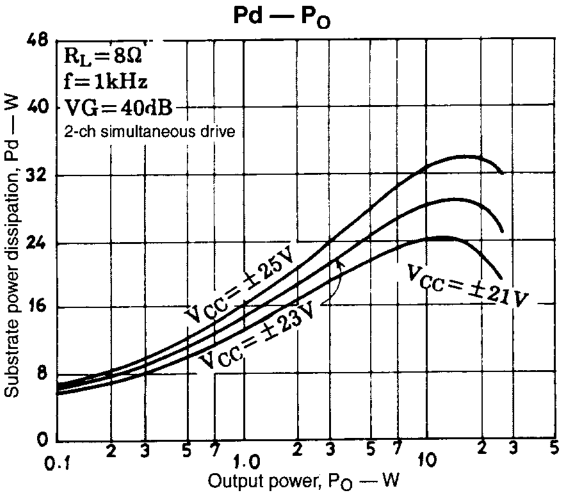


Figure 1. Pd – P_O (R_L=8Ω)

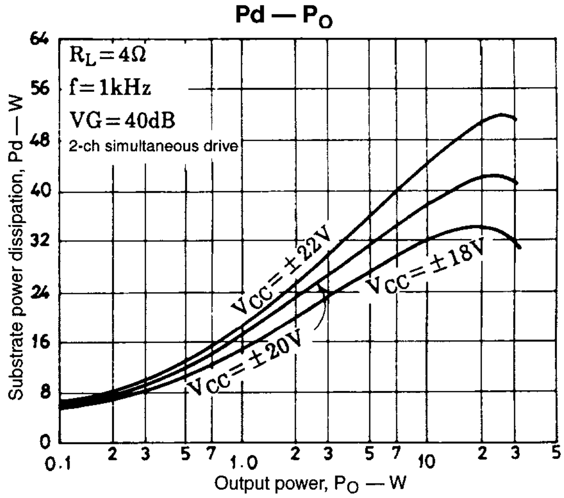


Figure 2. Pd – P_O (R_L=4Ω)

When estimating the power dissipation for an actual audio signal input, the rule of thumb is to select Pd corresponding to (1/10) × P_O max (within safe limits) for a continuous sine wave input. For example,

Pd=18.6W for 8Ω, and Pd=23W for 4Ω

The heatsink thermal resistance, θj-a, required to dissipate the STK41322 device total power dissipation, Pd, is determined as follows :

Condition 1: IC substrate temperature not to exceed 125°C

T_C=Pd×θc-a+Ta<125°C .... (1)

where Ta is the guaranteed maximum ambient temperature.

Condition 2: Power transistor junction temperature, Tj, not to exceed 150°C

Tj=Pd×θc-a+Pd/4×θj-c+Ta<150°C .... (2)

The STK4132 Ⅱ has 4 power transistors (2 per channel), and the thermal resistance per transistor, θj-c, is 3.0°C/W. Therefore, equation 2 becomes :

Pd× (θc-a+3.0/4)+Ta<150°C .... (3)

The required heatsink must have a thermal resistance that satisfies both expressions 1 and 3. Figure 3 shows the ambient temperature parameter against Pd and θj-a calculated from equations 1 and 3.

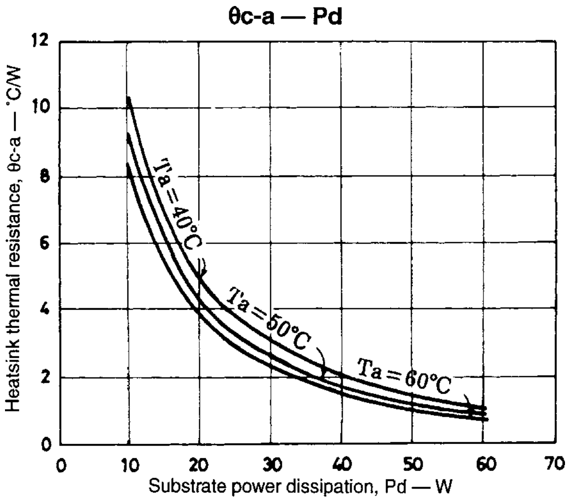


Figure 3. θc-a – Pd

For example, a stereo amplifier with ambient temperature of Ta=50°C needs a heatsink with thermal resistance given by the following :

For V_{CC}=±23V, R_L=8Ω :
1/10 P_O max corresponds Pd1=18.6W
From figure 3, the STK4132 Ⅱ thermal resistance is θc-a1=4.01°C/W
From equation 3, this results in a junction temperature Tj=139.1°C

For V_{CC}=±20V, R_L=4Ω :
1/10 P_O max corresponds Pd2=23W
From figure 3, the STK4132 Ⅱ thermal resistance is θc-a2=3.26°C/W
From equation 3, this results in a junction temperature Tj=142.3°C

This catalog provides information as of October, 1999. Specifications and information herein are subject to change without notice.